Amendments to the Specification:

Please replace the paragraph beginning at page 6, line 3 with the following amended paragraph:

When the object moves relative to the imaging device, however, the prolonged exposure imaging is not feasible because the captured image can be "smeared" when the exposure time is too long and the photons from one location of the object are collected by two or more adjacent pixels along the direction of the relative motion. The simple addition of multiple frames suffers the smearing problem since different frames are taken at different times and the image of the object has moved from one location **[[one]]** **on** the sensing array to another location during that time.

Please replace the paragraph beginning at page 7, line 1 with the following amended paragraph:

FIG. 1A illustrates the above time-delayed integration technique by using an aircraft-mounted imaging array device **to** take images of a ground scene. Seven consecutive frames taken by the imaging device are shown. Due to the motion of the aircraft, the ground scene projects at different locations on the imaging array along the direction of motion. However, if the frames are spatially shifted by one pixel between any two consecutive frames, the sensing pixels in the different frames

with the same ground scene are aligned and hence can be added to form the proper integrated image without smearing.

Please replace the paragraph beginning at page 8, line 10 with the following amended paragraph:

The APS array 110 may be formed **with** CMOS-compatible active pixel sensors integrated on a semiconductor substrate. The integrators may also be integrated with the APS array 110 on the same substrate by using the CMOS technology to perform the time-delayed integration. Such a CMOS imaging device hence can combine the time-delayed integration mechanism with various advantages and on-chip processing functionalities of the CMOS APS technology. Since each APS pixel internally converts the photon-induced charge into an electrical signal. Charge transfer from one pixel to another is avoided.

Please replace the paragraph beginning at page 14, line 7 with the following amended paragraph:

Another feature of the device 100 is to reduce the noise such as offsets and parasitic effects in the signal processing. The correlated double sampling mechanism of the APS array 110 significantly reduces the noise from the APS array 110. However, the time-delayed integration operation and the presence of the integrator array **[[130]]** **120** also raise additional noise

problems such as offsets and parasitic effects inherent in the integrators.

Please replace the paragraph beginning at page 14, line 15 with the following amended paragraph:

Those and other issues are addressed in the design of the integrator array **[[130]]** **120**. In particular, special switched-capacitor integrators are implemented to reduce the additional noise. The following are several exemplary designs of the integrator array 120.

Please replace the paragraph beginning at page 22, line 11 with the following amended paragraph:

The devices shown in FIGS. 3A and 5A still **[[has]]** **have** a residual offset even though both can cancel opamp offsets during every summing operation. This residual offset is introduced in the integrator reset phase when the input and the output of the opamp are connected together to provide the initial level $\left(V_0^+ \text{ and } V_0^+\right)$. In this process, the charges stored on the feedback capacitors are completely removed. This offset can be also be reduced by carrying out the integrator reset with one end of the feedback capacitor connected to the opamp input, and the other end connected to V_{cm}. This ensures that the offset is stored in the capacitor and is exactly cancelled in the subsequent phases.

Nor more switches are necessary, since each feedback capacitor is connected to V_{cm} through a switch anyway.